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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,457	07/29/2003	Kayoko Shibata	P/126-222	9037
2352	7590	06/29/2004	EXAMINER	
OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			NGUYEN, DANG T	
			ART UNIT	PAPER NUMBER
			2178	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/630,457	SHIBATA ET AL.
	Examiner Dang T Nguyen	Art Unit 2178

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 July 2003.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1,3-8,10-13, and 15 is/are rejected.
 7) Claim(s) 2,9 and 14 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 29 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 7/29/03.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: Search history.

DETAILED ACTION

1. This action is responsive to the following communications: the Application and The Information Disclosure Statement filed on July 29, 2003.
2. Claims 1-15 are pending in this case. Claims 1 and 8 are independent claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-8, 10-13, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Funaba et al. U.S. Patent No. 6,411,539 B2 – filed Mar. 12, 2001.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Regarding independent claim 1, Fig. 11 of Funaba et al. discloses a memory module for being inserted in any one of connectors formed on a motherboard,

comprising: a memory chip; a pin for being connected to the connector (Fig. 11); a bus [BUS] for connecting said memory chip to said pin; a terminating resistor [TERMINAL RESISTOR] connected to one end of said bus, and a stab resistor [TUB RESISTORS] connected between said pin and the other end of said bus (Col. 14 lines 24 – 29).

Regarding dependent claim 3, Fig. 11 of Funaba et al. further comprises other memory chips, wherein said bus is connected to all of the memory chips in common.

Regarding dependent claim 4, Fig. 11 of Funaba et al. further comprising other memory chips, other pins corresponding to said other memory chips respectively, and other buses for connecting said memory chips to said other pins severally.

Regarding dependent claims 5 and 6, even though Funaba et al. are silent to wherein the bus comprises either a bi-directional bus or a unidirectional bus. However the series bus line for memory module taught by Funaba et al. (Fig. 11) must be either a unidirectional or a bi-directional.

Regarding dependent claim 7, Fig. 17 of Funaba et al. discloses wherein said terminating resistor [106] is formed in said memory chip.

Regarding independent claim 8, the claim incorporated substantially same subject matter as of claim 1, and is rejected along the same rationale.

Regarding dependent claim 10, the claim incorporated substantially same subject matter as of claim 3, and is rejected along the same rationale.

Regarding dependent claim 11, the claim incorporated substantially same subject matter as of claim 3, and is rejected along the same rationale.

Regarding dependent claims 12 and 13, the claims incorporated substantially same subject matter as of claims 5 and 6 respectively, and are rejected along the same rationale.

Regarding dependent claim 15, the claim incorporated substantially same subject matter as of claim 7, and is rejected along the same rationale.

Allowable Subject Matter

4. Claims 2, 9 and 14 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 2 and 9, in addition to other elements in the respective claim, the prior art '539' as applied to claims 1, and 8 above teaches a memory module having a stab resistor connecting between one end of the bus line and the pin, and other end of the bus line is connecting to a terminating resistor. However '539' fails to teach wherein the stab resistance (Rs) and the terminating resistance (Rterm) are given by :

$$Rs = (N - 1) \times Z_{effdimm}/N \text{ and}$$

$$Rterm = X Z_{effdimm}$$

where N represents the number of said connectors; and Zeffdimm, effective impedance of a memory chip arrangement portion consisting of said bus and said memory chip.

With respect to claim 14, in addition to other elements in the claim, the prior art '539' as applied to claims 1, and 8 above teaches a memory module having a stab resistor connecting between one end of the bus line and the pin, and other end of the bus line is connecting to a terminating resistor. However '539' fails to teach wherein the stab resistance (Rs) and the terminating resistance (Rterm) meet an equation of:

$$Zmb = (Rs + Zeffdimm) / N$$

where Zmb represents wiring impedance of said motherboard;

Zeffdim, effective impedance of a memory chip arrangement portion consisting of said bus and said memory chip; and N, the number of said memory module.

Prior art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McCall et al. Patent No. US 6,711,027 B2 Date of Patent: Mar. 23, 2004

Ramachandran et al. Patent No. US 6,522,165 B2 Date of Patent: Feb. 18, 2003

Park et al. Patent No. US 6,480,409 B2 Date of Patent: Nov. 12, 2002

Wu et al. Patent No. US 6,690,191 B2 Date of Patent: Feb. 10, 2004

Contact Information

6. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (703) 305-1673. Normal contact times are M-F, 8-4:30.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Heather Herndon, may be reached at (703) 308-5186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7239 (for formal communications intended for entry)

or:

(703) 746-7238 (for after-final communications)

Hand-delivered responses should be brought to

Crystal Park II, 2121 Crystal Drive

Arlington, VA, Fourth Floor (receptionist)



6/28/04

Dang Nguyen 6/23/2004

RICHARD ELMS
SUPPLY/ADVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800